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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
FOWLKES, ANDRE R

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>22 September 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-21</u> is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-21</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) <u>22-45</u> are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>02 November 2001</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All   b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9/22/03</u>.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

1.   Claims 1-21 are pending.

Election/Restrictions

2.   Restriction to one of the following inventions is required under 35 U.S.C. 121:

I.   Claims 1-21, drawn to a method, computer-readable medium and apparatus for identifying optimal data references for anticipatory prefetching using a 2-phase marking process, classified in class 717, subclass 158.

II.   Claims 22-45, drawn to a method, computer-readable medium and apparatus for identifying optimal array references for anticipatory prefetching by determining a function for the array subscript in terms of a loop index, classified in class 717, subclass 158.

3.   The inventions are distinct, each from the other because of the following reasons:

4.   Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)).

5.   In the instant case, invention I, as claimed does not require the particulars of invention II, as claimed, because a two-phase marking strategy is used to identify an optimal set of data references to be prefetched, without performing all of the techniques claimed in invention II. Invention II, as claimed does not require the particulars of invention I as claimed because optimal array references for anticipatory prefetching are identified using a function for the array subscript in terms of a loop index, without performing all of the techniques claimed in invention I.

6.   Invention I has separate utility such as identifying a set of data references for anticipatory prefetching that is optimal, in terms of the 2-phase marking algorithm. Invention II has separate utility such as identifying a set of data references for anticipatory prefetching, that is optimal, in terms of the array subscript/loop index function.

7.   During a telephone conversation with A. Richard Park of Park, Vaughan & Fleming, LLP on 9/15/04, a provisional election was made without traverse to prosecute the invention of Group I, consisting of claims 1-21. Affirmation of this election must be made by applicant in reply to this Office action. Claims 22-45 are withdrawn from further consideration by the examiner, under 37 CFR 1.142(b), as being drawn to a non-elected invention.

8.   Applicant is reminded that upon the cancellation of claims to a non-elected

invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one

or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by

a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

9.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10.   Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by

Santhanam.

As per claim 1, Santhanam discloses a **method for generating code to**

perform anticipatory prefetching for data references, (col. 3:47-49, "The current

invention provides a new compiler for such a processor that facilitates efficient insertion

of explicit data prefetch instructions into loops within application programs"),

comprising:

     - receiving code to be executed on a computer system; analyzing the code

to identify data references to be prefetched, (col. 3:50-51, "The compiler uses ...

analysis (techniques) to determine data prefetching requirements"), **wherein analyzing the code involves:**

- performing a first marking phase in which only data references located in blocks that are certain to execute are considered in determining which data references are covered by preceding data references (col. 17:25-30, "a two-pass strategy is used... In the first pass, it is necessary to identify clusters of adjacent references... The distinguishing feature of each such cluster is that the references within the cluster share group spatial locality (i.e. data references that cover each other are determined)", and col. 12:18-22, "(Only) memory references (that are certain to execute are) ... analyzed for data prefetching purposes"),

- performing a second marking phase in which data references that are located in blocks that are not certain to execute are considered (col. 18:39-41, "Having identified the cluster leaders (i.e. the preceding references that cover other references), in the first pass, in the second pass, the algorithm attempts to exploit temporal locality between the clusters (i.e. references)", and col. 14:6-7, "Now it is also necessary to address the issue of loops that have internal branches"),

- inserting prefetch instructions into the code in advance of the identified data references (col. 3:51-53, "Analysis and explicit data cache prefetch instruction insertion are performed by the compiler").

As per claim 2, the rejection of claim 1 is incorporated and further, Santhanam discloses:

- profiling execution of the code to produce profiling results (col. 14:8-10, "using previously collected execution profile information, which indicates the execution count for each basic block"),

- using the profiling results to determine whether a given block of instructions is executed frequently enough to perform the second marking phase on the given block of instructions (col. 14:6-10, "Now, it is also necessary to address the issue of loops that have internal branches. The minimum loop iteration latency for such loops is estimated by using previously collected execution profile information, which indicates the execution count for each basic block in the loop body.").

As per claim 3, the rejection of claim 2 is incorporated and further, Santhanam discloses that **determining whether the given block of instructions is executed frequently enough to perform the second marking phase involves comparing a frequency of execution for the given block from the profiling results with a threshold value indicating a minimum frequency of execution to be considered in the second marking phase** (col. 12:18-22, "(Only) memory references with (a minimum stride value) … are further analyzed for data prefetching purposes").

As per claim 4, the rejection of claim 1 is incorporated and further, Santhanam discloses that analyzing the code involves **identifying loop bodies within the code and identifying data references to be prefetched from within the loop bodies** (col. 8:30-35, "One important feature of the invention identifies loops and access patterns to

allow a determination of how many cycles are devoted to loop iterations, and therefore

allows insertion of the prefetch instruction(s)").

As per claim 5, the rejection of claim 4 is incorporated and further, Santhanam

discloses that **if there exists a nested loop within the code,** (col. 16:60, "consider the

following 'C' loop nest"), **analyzing the code involves:**

- **examining an innermost loop in the nested loop** (col. 17:5-6, "(the) inner j-

loop (is examined)"),

- **examining a loop outside the innermost loop if the innermost loop is**

smaller than a minimum size or is executed fewer than a minimum number of

iterations (col. 17:8-9, "It must be determined whether it is sufficient to insert only one

prefetch instruction on behalf of (inner and outer loop references if the inner loop is

executed fewer than a minimum number of iterations").

As per claim 6, the rejection of claim 4 is incorporated and further, Santhanam

discloses that **analyzing the code to identify data references to be prefetched**

involves examining a pattern of data references over multiple loop iterations (col.

14:7-10, "(Data references to be prefetched are identified) by using previously collected

execution profile information, which indicates the execution count for each basic block in

the loop body.").

As per claim 7, the rejection of claim 1 is incorporated and further, Santhanam discloses that **analyzing the code involves analyzing the code within a compiler** (col. 3:47-49, "The current invention provides a new compiler for such a processor that facilitates efficient insertion of explicit data prefetch instructions into loops within application programs").

As per claims 8-14, this is a computer readable medium/product version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Santhanam's new compiler (col. 3:47-49).

As per claims 15-21, this is an apparatus version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Santhanam Fig. 1 item 10, "computer architecture" and associated text.

Conclusion

11.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre R. Fowlkes whose telephone number is (703)305-8889. The examiner can normally be reached on Monday - Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Tuan Q. Dam can be reached on (703)305-4552. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

12.   After October 25, 2004, the examiner can be reached at new telephone number

(571) 272-3697, and the examiner's supervisor, Tuan Q. Dam can be reached on (571)

272-3695.

ARF

TUAN DAM
SUPERVISORY PATENT EXAMINER